AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously presented) A method for latching and amplifying a capacitively coupled inter-chip communication signal, comprising:

receiving an input signal on a capacitive receiver pad from a capacitive transmitter pad;

feeding the input signal through an inverter to produce an output signal;

feeding the output signal through a weakened inverter to produce a feedback signal;

feeding the feedback signal back into an input of the inverter so as to form a latch for the input signal between the inverter and the weakened inverter; and

establishing a high bias voltage, V_H, with a high bias voltage generator and establishing a low bias voltage, V_L, with a low bias voltage generator;

wherein the high bias voltage generator includes a mechanism for adjusting the high bias voltage, V_H;

wherein the low bias voltage generator includes a mechanism for adjusting the low bias voltage, V_L;

wherein the weakened inverter is biased to produce the feedback signal that swings between the high bias voltage, V_H, and the low bias voltage, V_L; and

wherein V_H is slightly higher than a switching threshold of the inverter, and V_L is slightly lower than the switching threshold of the inverter, whereby the feedback signal causes the input signal to reside within a narrow voltage range

near the switching threshold of the inverter, thereby making the inverter sensitive to small transitions in the input signal received on the capacitive receiver pad.

2. (Original) The method of claim 1, further comprising amplifying an output of the inverter through an amplification stage to produce an amplified output signal.

3-4 (Canceled).

5. (Previously presented) The method of claim 2, further comprising adjusting the high bias voltage generator and the low bias voltage generator to provide a specified sensitivity to transitions of the input signal.

6. (Previously presented) The method of claim 2, further comprising adjusting the high bias voltage generator and the low bias voltage generator to provide a specified noise immunity to noise associated with the input signal.

7 (Canceled).

8. (Previously presented) An apparatus for latching and amplifying a capacitively coupled inter-chip communication signal, comprising:

a receiving mechanism configured to receive an input signal on a capacitive receiver pad from a capacitive transmitter pad;

a latching mechanism configured to feed the input signal through an inverter to produce an output signal; and

a biasing mechanism configured to establishing a high bias voltage, V_H, with a high bias voltage generator and establishing a low bias voltage, V_L, with a low bias voltage generator;

wherein the high bias voltage generator includes a mechanism for adjusting the high bias voltage, V_H;

wherein the low bias voltage generator includes a mechanism for the low bias voltage, V_L;

wherein the latching mechanism is further configured to feed the output signal through a weakened inverter to produce a feedback signal;

wherein the latching mechanism is further configured to feed the feedback signal back into an input of the inverter so as to form a latch for the input signal between the inverter and the weakened inverter;

wherein the weakened inverter is biased to produce the feedback signal that swings between the high bias voltage, V_H, and the low bias voltage, V_L; and

wherein V_H is slightly higher than a switching threshold of the inverter, and V_L is slightly lower than the switching threshold of the inverter, whereby the feedback signal causes the input signal to reside within a narrow voltage range near the switching threshold of the inverter, thereby making the inverter sensitive to small transitions in the input signal received on the capacitive receiver pad.

9. (Original) The apparatus of claim 8, further comprising an amplifying mechanism configured to amplify an output of the inverter through an amplification stage to produce an amplified output signal.

10-11 (Canceled).

12. (Previously presented) The apparatus of claim 9, further comprising an adjusting mechanism configured to adjust the high bias voltage generator and the low bias voltage generator to provide a specified sensitivity to transitions of the input signal.

13. (Previously presented) The apparatus of claim 9, further comprising an adjusting mechanism configured to adjust the high bias voltage generator and the low bias voltage generator to provide a specified noise immunity to noise associated with the input signal.

14 (Canceled).

15. (Previously presented) A means for latching and amplifying a capacitively coupled inter-chip communication signal, comprising:

a receiving means for receiving an input signal on a capacitive receiver pad from a capacitive transmitter pad;

a latching means configured to feed the input signal through an inverter to produce an output signal; and

a biasing means for establishing a high bias voltage, V_H, with a high bias voltage generator and for establishing a low bias voltage, V_L, with a low bias voltage generator;

wherein the high bias voltage generator includes a mechanism for adjusting the high bias voltage, V_H; and

wherein the low bias voltage generator includes a mechanism for the low bias voltage, V_L;

wherein the latching means is further configured to feed the output signal through a weakened inverter to produce a feedback signal;

wherein the latching means is further configured to feed the feedback signal back into an input of the inverter so as to form a latch for the input signal between the inverter and the weakened inverter;

wherein the weakened inverter is biased to produce the feedback signal that swings between the high bias voltage, V_H, and the low bias voltage, V_L; and

wherein V_H is slightly higher than a switching threshold of the inverter, and V_L is slightly lower than the switching threshold of the inverter, whereby the feedback signal causes the input signal to reside within a narrow voltage range near the switching threshold of the inverter, thereby making the inverter sensitive to small transitions in the input signal received on the capacitive receiver pad.

16. (Original) The means of claim 15, further comprising an amplifying means for amplifying an output of the inverter through an amplification stage to produce an amplified output signal.

17-18 (Canceled).

19. (Previously presented) The means of claim 16, further comprising an adjusting means for adjusting the high bias voltage generator and the low bias voltage generator to provide a specified sensitivity to transitions of the input signal.

20. (Previously presented) The means of claim 16, further comprising an adjusting means for adjusting the high bias voltage generator and the low bias voltage generator to provide a specified noise immunity to noise associated with the input signal.

21 (Canceled).

22. (New) The method of claim 1, further comprising adjusting an *RC* time constant for the feedback signal so that the time constant for the feedback signal is significantly larger than the time constant for the transmitted signal from the

capacitive transmitter pad, thereby ensuring that the feedback signal does not mask transitions of the transmitted signal.

23. (New) The apparatus of claim 8, further comprising an adjusting mechanism configured to adjust an *RC* time constant for the feedback signal so that the time constant for the feedback signal is significantly larger than the time constant for the transmitted signal from the capacitive transmitter pad, thereby ensuring that the feedback signal does not mask transitions of the transmitted signal.

24. (New) The means of claim 15, further comprising an adjusting means for adjusting an *RC* time constant for the feedback signal so that the time constant for the feedback signal is significantly larger than the time constant for the transmitted signal from the capacitive transmitter pad, thereby ensuring that the feedback signal does not mask transitions of the transmitted signal.